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Wide-Bandgap Device Enabled Multilevel Converters With Simplified Structures and Capacitor Voltage Balancing Capability

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ABSTRACT This paper aims to point out and demonstrate the opportunities enabled by wide-bandgap (WBG) devices for multilevel converters, contributing to the international technology roadmap for WBG power semiconductors (ITRW). The emergence of silicon carbide (SiC) and gallium nitride (GaN) devices offers new opportunities to push the boundaries of power converter performances. Featuring high single-device blocking voltage and ultra-low switching loss, WBG devices can enable a group of multilevel converters with simplified structures and a higher number of levels to be practically implemented in applications with various power levels. This paper highlights how the use of WBG devices can reduce the number of required devices in the simplified multilevel topologies, how the capacitor voltage balance can be achieved with the newly proposed redundant level modulation (RLM) enabled by the ultra-low switching loss of WBG devices and how the switching frequency and efficiency can be improved with WBG multilevel converters. A 1.2 kV/100 kW, three-phase demonstrator implemented with a simplified four-level active neutral point clamped (ANPC) structure and commercial SiC power modules is studied to show the opportunities brought by WBG devices for multilevel converters. A voltage balancing scheme based on the RLM and a power loss analysis are presented for this configuration.

INDEX TERMS Wide-bandgap, silicon carbide (SiC), multilevel converters, reduced device count, capacitor voltage control, redundant level modulation.

I. INTRODUCTION

Wide-bandgap (WBG) power devices developed over the past decades, such as silicon carbide (SiC) and gallium nitride (GaN) devices, offer new opportunities pushing the boundaries of power converter performances [1]. Alongside the development of power devices, multilevel converter topologies have also been an extensively studied topic since the 1960s, from the well-known neutral point clamped (NPC) converters, flying capacitor converters and cascaded H-bridge converters, to T-type converters, active-NPC (ANPC) converters and modular multilevel converters (MMC) [2], [3]. One motivation for the invention of multilevel converters is to offer higher voltage handling capability [4], considering the limited device blocking voltage for medium voltage or high voltage applications. Another motivation for developing multilevel converters is the benefits to the power density and efficiency in lower-voltage applications [4], [5], which is a result of reduced filtering requirement due to lower harmonics [6] and lower switching loss due to lower switching voltage [7], i.e., a fraction of the full dc-link voltage. Nowadays, researchers are still actively deriving multilevel topologies with more voltage levels (e.g., four levels or more) [2], [3] to cope with the trend of higher voltage systems (e.g., 800 V dc instead of 400 V dc, medium voltage instead of low voltage due to increased power demand in various applications), while mitigating the impact on converter performance caused by the higher switching voltage and switching loss, which is justified in the scaling law for multilevel converters presented in [8]. The pursuit of

a higher number of voltage levels is further driven by further reduction of dv/dt, electro-magnetic interference (EMI) and filtering requirement.

There seems to be a good marriage between multilevel converters and WBG devices, which brings in new opportunities. For example, the fast switching speed of WBG devices, while reducing the switching losses, results in significant voltage stress (dv/dt) and EMI related issues. Fortunately, multilevel converters have natural low dv/dt and low EMI. Therefore, using WBG devices in multilevel converters can bring in low switching loss with mitigated negative side-effects of dv/dt and EMI. For GaN HEMTs, albeit their super-fast switching speeds, e.g., <10 ns turn-on/off time, the limited voltage rating of <650 V means they only have restricted use for application with a dc-link voltage lower than 400 V if employed in a standard two-level converter. Again, fortunately, multilevel converters provide an effective way to extend their use for applications with a dc-link voltage higher than 400 V. On the other hand, the WBG devices will also benefit multilevel converters regarding simplified topologies and capacitor voltage balancing capability.

One of the common drawbacks with multilevel converters in various applications is their large number of switching devices and associated gate drive circuits, protection circuits, failure possibility, etc. To tackle this bottleneck of multilevel converters and to further improve their performance, a group of simplified topologies and higher-number-of-level topologies have been actively derived and researched as alternatives [2], [9], [10]. The logic of topology simplification is to employ fewer devices (i.e., fewer power semiconductors and capacitors) while achieving the same voltage levels and output converter performance. To achieve reduced device count, the common penalty is the increased blocking voltage for part of the power devices. For example, as a simplified topology to the three-level NPC converter [11], the T-type converter [12] removes two diodes in one phase leg while the two switches in the main leg need to block the full dc-link voltage instead of half the dc-link voltage. To achieve more voltage levels, apart from the increased number of devices, the typical challenge is the increased difficulties of balancing the capacitor voltages. For example, derived from three-level NPC topologies, the four-level (4L) NPC topologies [2], [13] all features the challenging voltage balancing issue that cannot be completely solved by the conventional approaches based on zero-sequence signal injection in carrier-based modulation [14] or redundant vectors in space vector modulation [13]. Although there are novel approaches proposed recently to address this issue, they mandatorily utilize redundant levels [15] and require an increased number of switching events (e.g., up to +100 %) as the penalty of gaining extra controllability, which significantly increases the switching loss and undermines the benefit as a multilevel topology.

Fortunately, SiC devices bring new opportunities for this group of multilevel topologies because of their higher single-device blocking voltage (e.g., 10+ kV in SiC MOSFETs and 15+kV in SiC IGBTs, in contrast to 6.6 kV in Silicon (Si) IGBTs) [16] and significantly lower switching losses. These two features of SiC devices exactly combat the two weaknesses (i.e., higher voltage rating device and capacitor voltage balancing) mentioned above in simplified and higher-number-of-level topologies, which can enable these topologies to be practically implemented. Combining the SiC devices and advanced multilevel topologies can be expected to further improve the performances of power electronics converters in terms of voltage handling capability, lower harmonics, lower EMI and higher density and efficiency. While this paper focuses on SiC multilevel converters, the above is also true for GaN-device-based multilevel converters in a lower voltage application. The above opportunities created by WBG-device-based multilevel converters are applicable for various power levels including low voltage (LV), medium voltage (MV) and high voltage (HV) operation for the benefit of reducing the number of switching devices and reducing the switching losses, output harmonics (filtering), dv/dt, etc.

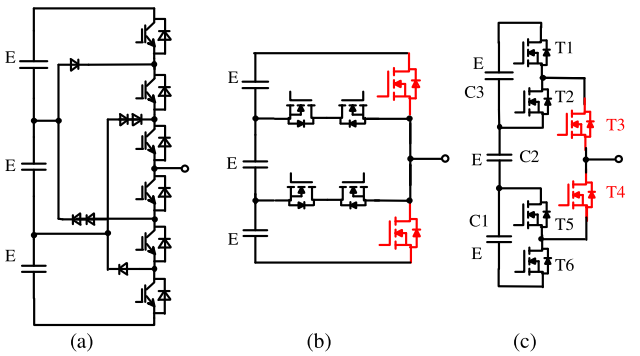

FIGURE 1. Conventional and simplified four-level converter topologies, (a) 4L diode NPC, (b) 4L π-type [9], and (c) 4L-ANPC [17].

The contribution of this paper is to demonstrate how WBG devices can enable and benefit a group of simplified multilevel topologies, with an example of a 1.2 kV demonstrator realized with a simplified four-level topology and commercial SiC power modules. To enable the simplified topology to operate without losing internal voltage balance, a voltage balancing scheme based on redundant level modulation is developed to factor in its impacts on device power losses. To demonstrate the benefits of SiC devices, a quantified device loss analysis is conducted against commercial Si counterparts.

II. OPPORTUNITIES OF SiC DEVICES IN SIMPLIFIED MULTILEVEL CONVERTER TOPOLOGIES

This section elaborates on the challenges in simplified multilevel structures with a higher number of levels in terms of device voltage requirement and voltage balancing capability. Fig. 1 shows three four-level converter examples. Fig. 1(a) is the conventional diode NPC converter. Fig. 1(b) is the four-level π-type converter [9]. And Fig. 1(c) is the four-level ANPC converter [17]. While the conventional diode NPC needs 6 additional clamping diodes, the latter two simplified topologies only need 6 devices in total per phase leg, which is

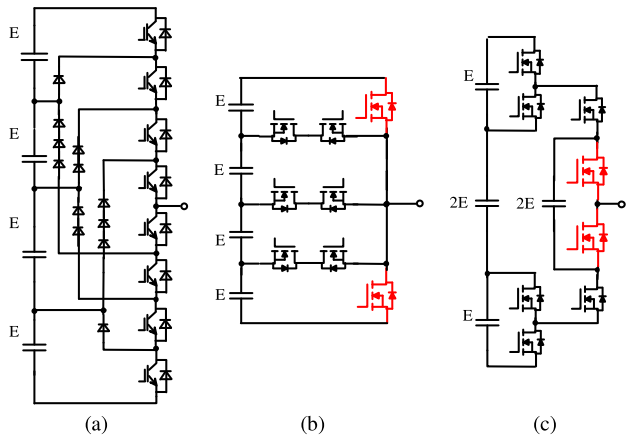

FIGURE 2. Simplification of five-level topologies, (a) 5L diode NPC, (b) 5L E-type [18], and (c) 5L-ANPC [2].

a clear advantage from the device count point of view. Fig. 2 shows the conventional diode NPC five-level (5L) converter as well as two simplified five-level topologies. Again, with the simplified topologies, the number of power devices is reduced. How these simplified topologies can be derived/obtained was given in [2].

However, as the penalty, the simplification of multilevel topologies also brings challenges regarding the device voltage requirement and voltage balancing issue, which are elaborated as follows.

A. DEVICE VOLTAGE REQUIREMENT

Here, the simplified four-level topologies given in Fig. 1(b)(c) are used as examples. For the four-level π-type converter, the two outer devices (marked in red) need to block the full dc-link voltage in static, rather than 1/3 of the dc-link voltage as the switching devices in the conventional diode NPC in Fig. 1(a). For example, when the upper red switch is turned ON, the lower red switch will see the full dc-link voltage of 3E. This increases the device voltage rating requirement for these two devices inside the topology, so these topologies in the past can only be considered for use in relatively low voltage applications given the limit of the voltage rating of Si devices. Similarly, for the topology in Fig. 1(c), T3 and T4 need to block 2/3 of the dc-link voltage, rather than 1/3 in conventional topologies. The fundamental reason why these devices need to block higher voltages than the rest of the devices was explained in [2], i.e., they represent two devices in series in the topology from which it is derived. This drawback prevented these simplified topologies to be implemented in higher-voltage systems in the past, as the increased blocking voltage exceeds the limit of the Si devices.

Fortunately, SiC devices offer higher possible blocking voltages that can counter this disadvantage of higher voltage requirement in these simplified multilevel topologies. It should also be noted that although T3 and T4 need to block a higher voltage, the actual switching devices used in these places do not need to have a large voltage safety margin

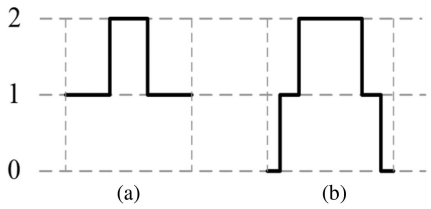

FIGURE 3. Illustration of (a) conventional PWM patterns and (b) the patterns for redundant level modulation. 0, 1, 2 represent three voltage levels.

because this high voltage is a static voltage requirement and the actual switching voltage is lower, i.e., 1/3 of the dc-link voltage for a four-level converter. Instead of using a switching device with a normal +100% voltage margin to account for the voltage overshoot during turn-off, a 20% voltage margin is enough for switching devices used for T3 and T4. Taking this into account, the emergence of 10 kV SiC MOSFETs makes it possible for the four-level π-type converter in Fig. 1(b) to sustain a dc-link voltage of around 8.3 kV. The 10 kV SiC MOSFET can enable the 4L-ANPC topology in Fig. 1(c) to sustain a dc-link voltage of 12.5 kV, corresponding to an AC output line rms voltage of 8.8 kV. This was not possible when there were only 6.6 kV Si IGBT modules.

B. VOLTAGE BALANCING REQUIREMENT AND IMPACT ON SWITCHING LOSS

The other challenge of NPC and simplified multilevel topologies with more voltage levels is the voltage balancing issue. For three-level converters, e.g., NPC or T-type, the dc-link capacitor voltages have a natural balancing capability over one fundamental cycle, e.g., for a 50Hz output frequency. And the capacitor voltage can also be actively controlled using zero-sequence signal injection (ZSI) in a carrier-based modulation or using redundant vectors in a space-vector-based modulation. However, for four-level topologies, such as the diode NPC topology in Fig. 1(a), the above two methods cannot keep the three dc-link capacitor voltages balanced, especially under high modulation indexes and higher power factors [13]. This is also true for simplified topologies in Fig. 1(b)(c). Although more complicated hybrid four-level converters such as the four-level hybrid clamped (4L-HC) converter [19] were proposed which can solve the capacitor voltage balancing issue, the cost is increased number of components.

To make 4L-ANPC and other simplified topologies usable with balanced capacitor voltages, novel modulation-based voltage balancing approaches have been proposed in [15], [20], [21], e.g., the redundant level modulation (RLM) proposed in [15]. Fig. 3 illustrates the switching pattern difference between the conventional zero-sequence injection or redundant vector based multilevel pulse width modulation (PWM) in Fig. 3(a) and the proposed redundant level modulation in Fig. 3(b), while they have the same volt-second product.

Essentially, the conventional PWM methods only allow the voltage to change one level within each switching period,

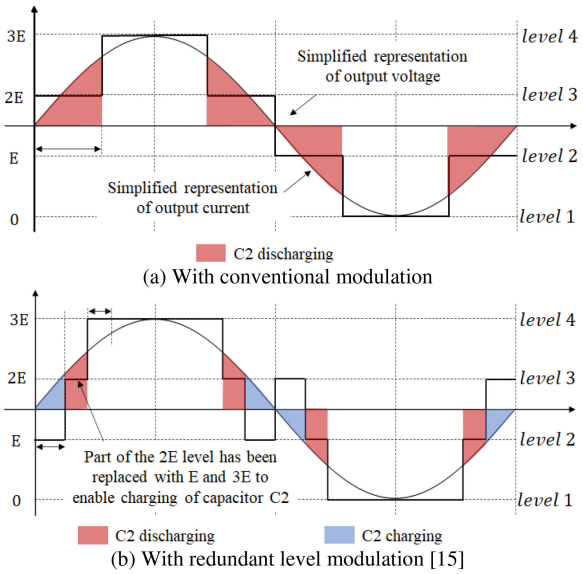

FIGURE 4. The output voltage and charge/discharge condition of the middle capacitor C2 in four-level NPC topologies. (a) With conventional modulation. (b) With redundant level modulation [15].

with one turn-on and one turn-off transition. The proposed redundant level modulation in Fig. 3(b) allows the voltage to change two or more levels in each switching period and there are four switching transitions i.e., 2 turn-ons and 2 turn-offs in this case, which leads to higher switching loss. This additional voltage level gives the extra controllability to regulate the dc-link capacitor voltages.

Fig. 4 illustrates the charge and discharge conditions of the dc-link middle capacitor C2 [15] shown in Fig. 1, which is the most difficult capacitor to control. With the conventional PWM, the capacitor C2 will keep discharge over one fundamental cycle, causing its voltage to diminish, as illustrated in Fig. 4(a). In contrast, with the proposed redundant level modulation, an additional voltage level can be used as illustrated in Fig. 4(b), which can balance the charge and discharge conditions of the capacitor C2, thus controlling its voltage to be 1/3 of the dc-link voltage as desired.

But, as the price, the RLM requires additional switching events to gain sufficient control to keep the four-level NPC and simplified topologies to operate normally without the capacitor voltages drifting away. The additional switching events (e.g., up to +100% [15]) lead to increased switching losses, which undermines the performance of these topologies. When it comes to a five-level NPC converter or other simplified topologies, it requires even more switching events to sufficiently balance the capacitor voltages [22], e.g., 6 switching transitions in one carrier cycle instead of 2 transitions in regular modulation. In other words, for these simplified multilevel topologies to be usable, the dc-link capacitors need to be infinitely large without utilizing the redundant output voltage levels. Otherwise, these topologies require external auxiliary voltage balancing circuits (such as in [18], [23]) that undesirably introduce extra devices and complexity. This mandatory drawback makes these simplified topologies less attractive in the context of last-generation Si devices due to the high switching losses.

Additionally, a well-balanced dc-link with low voltage ripples by using advanced control strategies (e.g., RLM) can reduce the required capacitance, hence reducing the cost and volume, and reliability concerns associated with the capacitors. A well-balanced dc-link can also reduce the voltage stress across the power devices, which otherwise may experience higher voltage transition and higher switching loss. If the dc-link voltage is not balanced, the output voltage waveforms will suffer higher harmonic distortions without showing the expected regular steps.

Fortunately, the ultra-low switching loss of WBG devices brings new opportunities for these simplified multilevel topologies with more voltage levels, which can moderate their drawback of mandatorily requiring more switching events to balance the capacitors and mitigate the increased switching losses. Therefore, this is the other reason that WBG can enable the implementation of these simplified multilevel topologies.

III. CASE STUDY: A 1.2 KV FOUR-LEVEL SiC DEMONSTRATOR

This section presents a case study of a 1.2 kV, 100kW, three-phase converter design employing a four-level simplified topology as shown in Fig. 1(c) and SiC power modules to demonstrate the advantages of using SiC devices in simplified converter topologies. As an advantage, this four-level ANPC topology can be formed by three half-bridge power modules in each phase without requiring additional clamping diodes. In this case, 1.7 kV SiC half-bridge power modules (CAS300M17BM2) and 1.2 kV SiC power modules (CAS300M12BM2) from Wolfspeed are selected. The 1.7 kV modules are used for devices T3 and T4 in Fig. 1(c) as they need to block a higher voltage. The 1.2 kV modules are used for devices T1&T2 and T5&T6. The dc-link voltage is designed at 1.2 kV to provide a higher voltage output than the standard 800 V dc-link to meet the increased voltage and power demand, e.g., in electric vehicle applications.

A. CONTROL STRATEGY FOR 4L-ANPC BASED ON RLM

As introduced, to enable the 4L-ANPC topology to be utilized as a single-end inverter, a special modulation scheme, RLM, is required to balance the capacitor voltages, especially the middle capacitor C2. Otherwise, under a high power factor, the C2 voltage will collapse to zero and the converter will lose the ability to provide the designed four-level operation if no auxiliary voltage balancing circuits are employed such as those in [23].

The RLM firstly proposed by the authors in [15] is adapted for the 4L-ANPC in this work, with its principles explained as follows. Following the concept shown in Fig. 3, the core concept of the RLM is to utilize additional voltage levels, e.g., three instead of two levels, to gain extra control of the capacitor voltages. As the basic principle, the RLM alters the high-frequency output voltage on a switching cycle basis

without altering the synthesized fundamental-frequency voltage, which is achieved by introducing an offset of duty ratios ΔD *as*

$$\begin{cases} D'_4 = D_4 + \Delta D \\ D'_3 = D_3 - 2\Delta D \ \ (V_{ref} \geq 0) \\ D'_2 = \Delta D \end{cases} \tag{1}$$

$$\begin{cases} D'_3 = \Delta D \\ D'_2 = D_2 - 2\Delta D \ \ (V_{ref} < 0) \\ D'_1 = D_1 + \Delta D \end{cases} \tag{2}$$

where D_4, D_3, D_2, D_1 are the original duty ratios of the four voltage levels derived from regular modulation; D'_4, D'_3, D'_2, D'_1 are the altered duty ratios obtained from RLM; V_{ref} is the reference voltage of a switching cycle. This duty ratio offset ΔD introduces one additional voltage level (e.g., *level 2* when $V_{\text{ref}} \geq 0$ and *level 3* when $V_{\text{ref}} < 0$), while the average output voltage (volt-second product) of the switching cycle remains the same. Meanwhile, the altered duty ratios (D'_3 and D'_2) lead to the closed-loop manipulation of the C2 voltage in one switching cycle as

$$\Delta V_{C2} = \frac{1}{3 \cdot C \cdot f_{sw}} \cdot \sum i_x \left(D'_{2x} - D'_{3x} \right) \tag{3}$$

where C is the capacitance of each capacitor in series; x represents the phase denotes ($x = a, b, c \ldots$); i is the load current.

Based on the above principles of RLM, a voltage balancing scheme for the 4L-ANPC topology is illustrated in Fig. 5.

Similar to the approach developed by the authors in [15], the easier control objective A, i.e., the balancing between two outer capacitors C1 and C3, is firstly solved by the conventional ZSI approach. Secondly, the balancing of C2 is solved by the RLM, which split into two cases depending on the polarity of the reference voltage. As illustrated in Fig. 5, the RLM operation can shrink the red discharge area for C2 and introduce the blue charge area to achieve the voltage balancing of C2. Note the RLM is implemented in each phase individually, which doubles the switching events in each switching cycle for all phases.

The control scheme is firstly developed and evaluated in simulation with passive RL load. Fig. 6 shows the performance of the proposed voltage balancing scheme for the 4L-ANPC, 1.2 kV inverter configuration.

As can be seen, the three capacitor voltages are well controlled at one-third of the dc-link voltage with only high-frequency ripples, even when the fundamental frequency f_0 is as low as 1 Hz. This excellent performance is a result of the proposed scheme realized in each switching cycle, which sufficiently controls all three capacitor voltages under the worst-case scenario (high M and high $cos\ \varphi$).

To verify the dynamic performance, Fig. 7 shows the waveforms in the simulation where the reference voltages of the three capacitors are individually stepped away from the nominal value.

As can be seen, both at a high and a low modulation index, the proposed scheme offers satisfying and seamless voltage

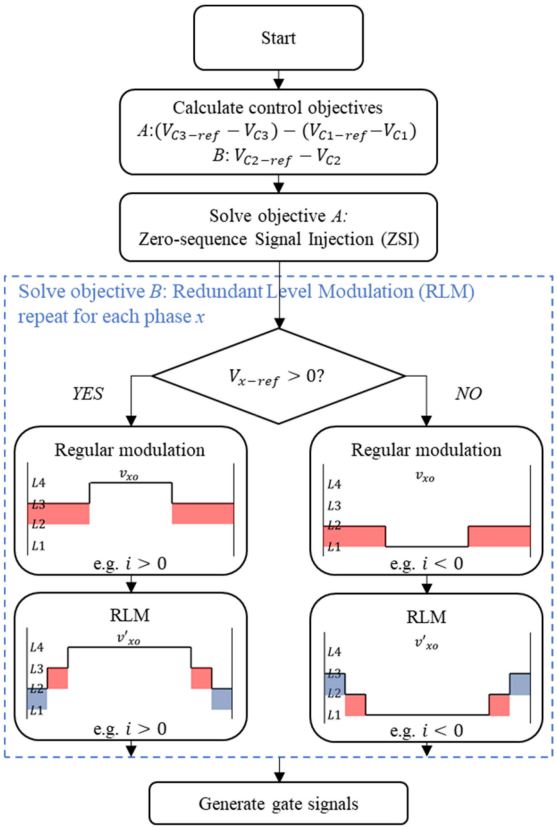

FIGURE 5. Proposed voltage balancing scheme for 4L-ANPC (illustrated in the case of unity power factor as the worst-case example).

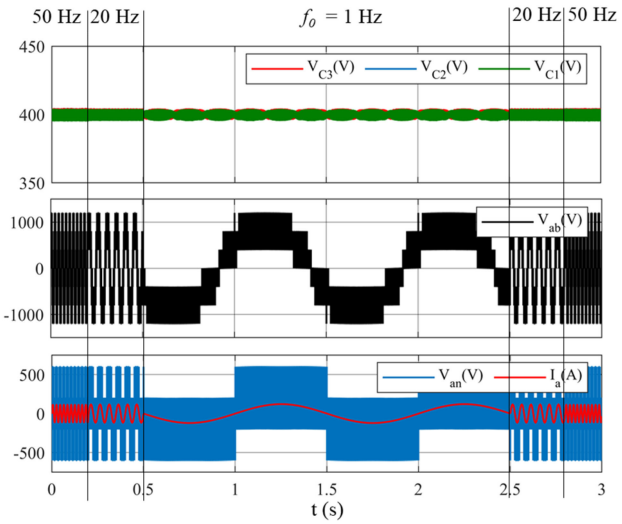

FIGURE 6. Performance under various fundamental frequency f_0 with M = 0.92, R = 4.57Ω, L = 3 mH (top: three dc-link capacitor voltages; middle: output line voltage; bottom: output phase voltage and load current).

balancing performance, not only tracking the reference values but also suppressing the ripples to high-frequency ripples only without any low-frequency distortions.

By performing FFT analysis, the harmonic contents and THD performance are shown in Fig. 8. Fig. 8(a) shows that the proposed converter system offers around 40% THD in the

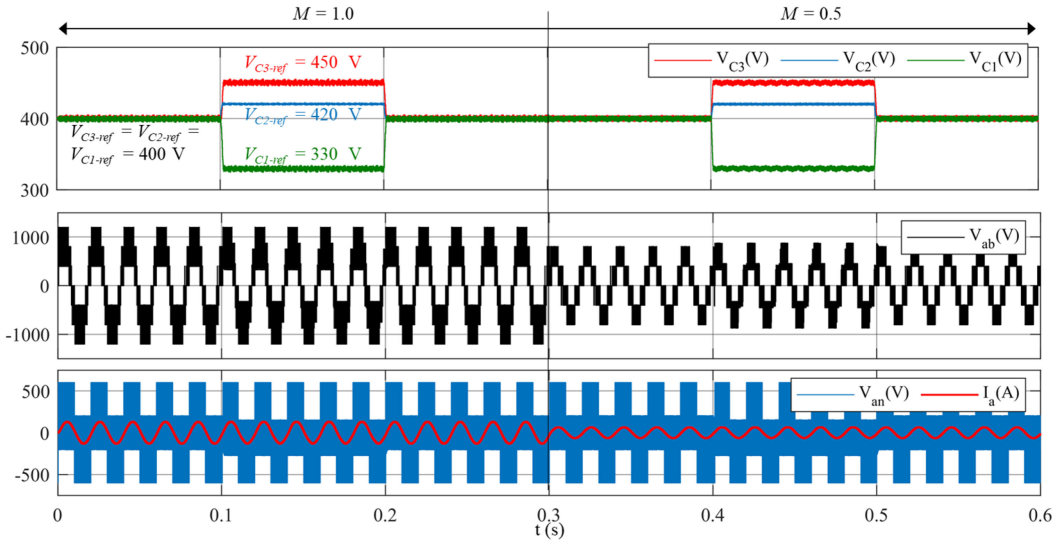

FIGURE 7. Dynamic control performance (top: three dc-link capacitor voltages; middle: output line voltage; bottom: output phase voltage and load current).

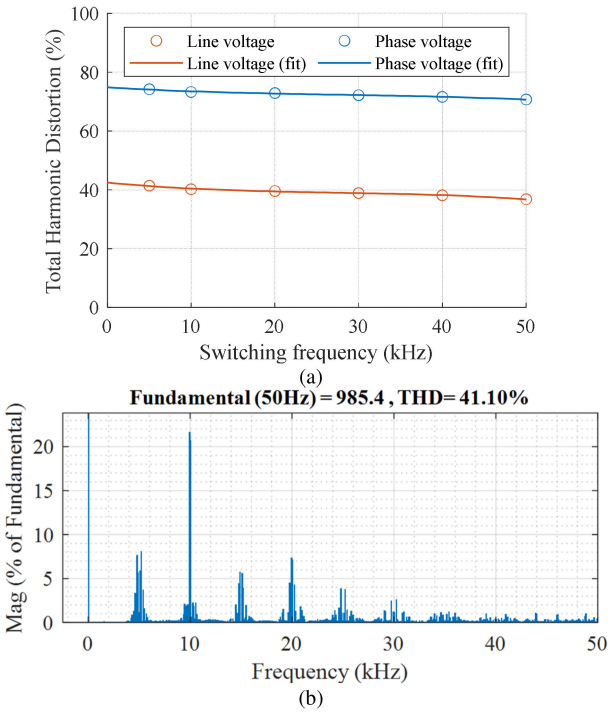

FIGURE 8. Harmonic performance. (a) THD (calculated up to 200 kHz) and (b) FFT of output line voltage at $f_{sw} = 5$ kHz.

output line voltage. Fig. 8(b) shows that the main harmonics locate at around the multiples of the switching frequency, especially at two times of f_{sw}, for which the RLM operation contributed to the increased amplitude compared to regular modulation. Regardless, the high-frequency harmonics are relatively easy to filter out, while there is no low-frequency harmonics since the RLM does not alter the low-frequency behaviour of the converter.

These simulation results prove the validity of the proposed voltage balancing scheme, which sufficiently enables the implementation of the 4L-ANPC topology.

B. POWER LOSS EVALUATION–Si VS. SiC DEVICES

This section evaluates the power device losses in the proposed system to demonstrate the benefits of SiC devices over the Si devices in the 4L-ANPC topology. Since the RLM is mandatory for the normal operation of the 4L-ANPC topology, its negative impact on the power device losses, i.e. the increased switching losses, should also be considered as the unavoidable running cost.

To provide a comparison, the commercial Si counterparts against the selected SiC modules are listed in Table 1 with their typical characteristics retrieved from manufacturer datasheets. The switching energies are all scaled linearly to 600 volts.

As can be seen, with the conduction performance similar to each other, the major advantage of the SiC power modules is the significantly lower switching energies of the MOSFET and the zero reverse-recovery energies of the diodes. This advantage is expected to significantly moderate the increased switching losses brought by the RLM.

Due to the complexity of the proposed RLM scheme, it is not feasible to analytically evaluate the power device losses as implemented in [24], [25]. Therefore, the power losses are modelled in simulation by Simulink/PLECS with the characteristics from the datasheets imported. The predicted converter efficiency is plotted in Fig. 9 against the switching frequency up to 50 kHz, with the synchronous conduction implemented for the SiC MOSFETs.

TABLE 1. Comparison of Si vs. SiC Power Devices (T_j = 150 °C)

	Voltage rating	Current rating	Power module		V_{FW0} (V)	R_{on} (mΩ)	V_{FW} (V) @300 A	E_{sw} (mJ) (600 V, 300 A)
Si	1200 V	300 A	SKM300GB12E4	IGBT	0.17	5.7	2.25	27 (ON) + 39 (OFF)
				Diode	0.9	4.0	2.11	23
	1700 V		SKM300GB17E4	IGBT	0.7	5.3	2.29	44 (ON) + 60.5 (OFF)
				Diode	1.08	3.5	2.13	38.5
SiC	1200 V		CAS300M12BM2	MOSFET	0	7.7	2.31	5.8 (ON) + 6.1 (OFF)
				Diode	0.75	4.2	2.0	0
	1700 V		CAS300M17BM2	MOSFET	0	16.2	4.86	8.7 (ON) + 6.6 (OFF)
				Diode	0.75	4.8	2.2	0

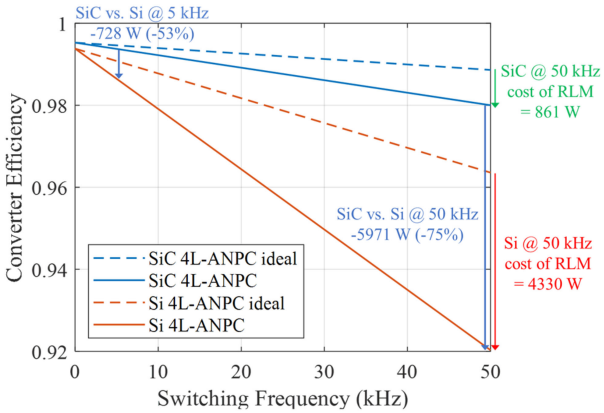

FIGURE 9. Converter efficiency.

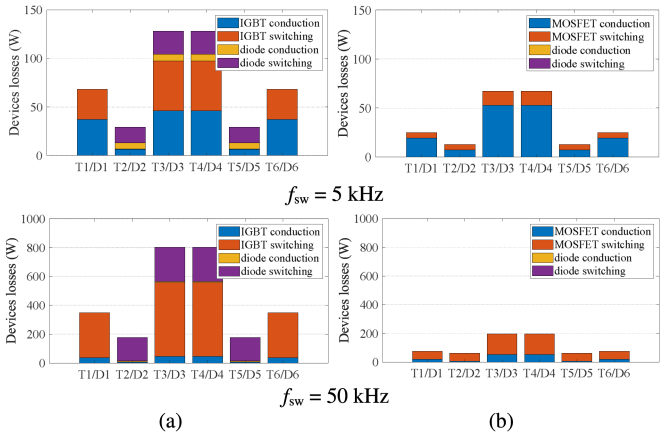

FIGURE 10. Device loss breakdown. (a) Si. (b) SiC.

As shown, operating at 100 kW and 1.2 kV, the proposed SiC converter (blue solid trace) can still maintain a **99.4%** efficiency at 5 kHz of switching frequency f_{sw}, as benefited from the multilevel topology (lower switching voltage, 400 V) and low switching loss of SiC MOSFETs. Note that this result already included the effect of increased switching events caused by the redundant levels [15] to balance the capacitor voltages. When the switching frequency f_{sw} is increased to 50 kHz, the converter can keep efficiency above **98%**.

In contrast, the Si solution (red solid trace) suffers from higher switching losses and the efficiency deteriorates quickly with the rise of switching frequency, which can only achieve the efficiencies of **98.6%** and **92.0%** at 5 kHz and 50 kHz, respectively. This means that the Si solution will suffer from significant cost in efficiency if the switching frequency is increased to shrink the filtering components.

In summary, by replacing Si devices with SiC devices, the proposed converter enjoys a loss reduction of 728 W at 5 kHz and 5971 W at 50 kHz.

To demonstrate the side effect of RLM, the power losses are also evaluated assuming an ideal dc-link (e.g., three ideal isolated dc supplies put in series) and regular sinusoidal PWM (SPWM) modulation as a reference with the results plotted as dashed lines, which is not feasible in reality. It can be seen that the RLM operation does lead to considerably higher switching losses (e.g., + 100%) as the cost of balancing the capacitor voltages. However, this cost is moderated by the SiC devices down to 861 W at 50 kHz in comparison to 4330 W in the Si case.

From the device point of view, a breakdown of power losses is illustrated in Fig. 10 under two switching frequency cases. As can be seen, the 4L-ANPC topology leads to around 60% of the power losses concentrated on the 1700 V power module T3/T4, while the other two 1200 V power modules each shares only 20% of the total power loss. This thermal unbalance between the power modules is considered as the characteristic of the topology and needs to be accounted for in the thermal design. In the 5 kHz case, the differences are 158 W and 97 W in the Si and SiC cases, respectively.

When the switching frequency is increased to 50 kHz, e.g., for reducing the size of the filter components, the switching loss become dominant and the high switching loss of the Si solution is amplified, which causes an unbalance of 1076 W between the 1700 V module and the 1200 V modules. Fortunately, this unbalance can be significantly improved by the SiC devices to 256 W only. Therefore, applying SiC devices can also benefit the 4L-ANPC topology in terms of moderating the thermal unbalance, especially in the case with a higher switching frequency.

C. DEMONSTRATOR AND EXPERIMENTAL VERIFICATION

As a proof of concept, a demonstrator is built and tested in a down-scaled experimental rig with 1 kV dc-link voltage input,

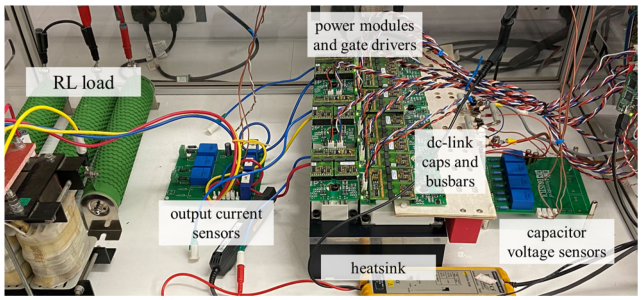

FIGURE 11. Downscaled test rig.

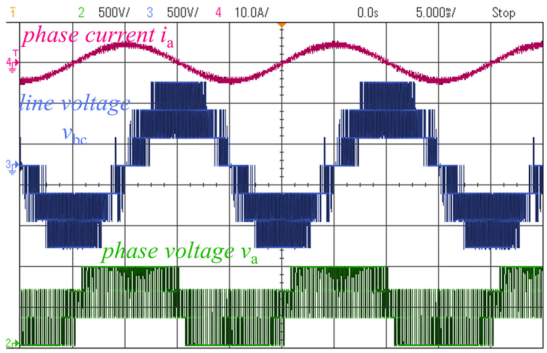

FIGURE 12. Experimental waveforms (phase voltage v_a referenced to the negative dc rail).

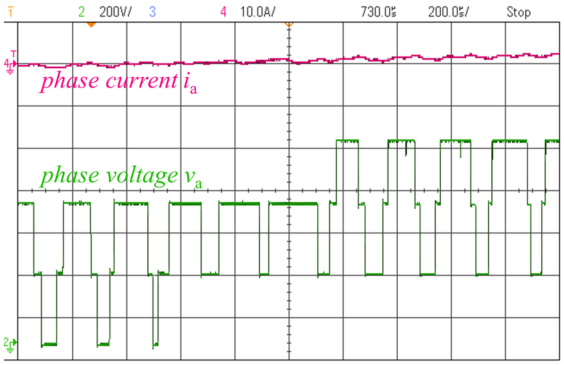

FIGURE 13. Zoomed-in view of measured phase voltage with RLM pattern.

switching frequency of 5 kHz, output frequency of 50 Hz, modulation index of 0.9 and 100 Ω/6.3 mH R-L load. The dc-link capacitors are selected at 450 μF so that the high-frequency dc-link capacitor voltage ripple is below 2% of dc-link votlage as evaluated in the simulation. Fig. 11 shows a picture of the test rig with the demonstrator mounted on an air-cooled heatsink and wired up with load and gate signals.

Running at 1 kV dc-link voltage, Fig. 12 shows the captured output current, line voltage and phase voltage of the converter. With the RLM voltage balancing [15] implemented, it can be seen in the phase voltage that the converter steadily outputs four voltage levels.

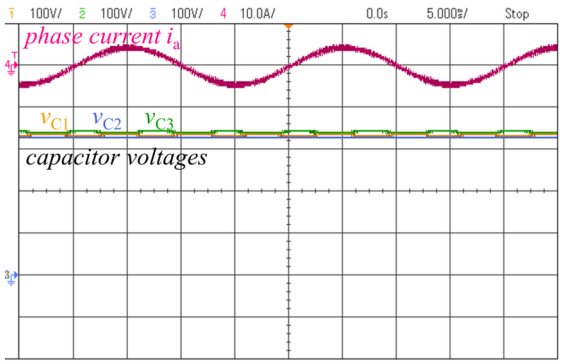

FIGURE 14. Measured voltage waveforms of three dc-link capacitors.

Fig. 13 shows a zoomed-in view of the phase voltage, with each time division of 200 μs equal to one switching cycle (f_{sw} = 5 kHz). As can be seen, the converter outputs three voltage levels with four switching transitions in some carrier cycles as intended by the RLM operation. The main side effect of this operation, the increased switching loss, is mitigated by the SiC devices.

Fig. 14 shows the steady-state waveforms of capacitor voltages. Thanks to the RLM scheme, the challenging voltage balancing issue is successfully solved in this topology, where all the three-link capacitor voltages are kept at 1/3 of the dc-link voltage of 333.3 V. Note the converter is operating at a high modulation index (M = 0.9) and a high power factor ($cos\ \varphi$ = 0.99) in this case, which is close to the worst-case scenario for capacitor voltage balancing in this simplified topology.

D. SUMMARY

To summarize, for a group of simplified multilevel converter topologies, the emerging WBG devices bring promising opportunities. The higher blocking voltage of WBG devices enables these topologies to be applied in an extended range of applications considering the voltage rating. The lower switching loss of WBG devices makes these topologies more attractive by mitigating the switching loss penalty of utilizing additional switching events to balance the internal capacitor voltages, which is in contrast to a substantially higher cost with the last-generation Si devices. These points are demonstrated in the presented case study as an example.

Although the cost of WBG devices is higher than the Si devices (around three times higher depending on the voltage/current ratings), due to the lower power loss (high efficiency), the converter heatsink can be smaller for WBG converters, thus reducing the heatsink/cooling cost. The switching frequency of WBG converters can also be higher, thus reducing the filtering/passive components and their cost. Overall, the cost of WBG converters is still higher than Si converters, but this is offset by the lower passive and cooling cost. On top of this, WBG devices can bring in efficiency, power density and other performance improvements which silicon converters cannot achieve.

IV. CONCLUSION

This paper has highlighted that WBG devices can enable and benefit the implementation of a group of simplified multilevel topologies with a higher number of levels for applications with various power levels. While reducing the required components, simplified multilevel topologies typically require higher blocking voltage of power devices and special voltage balancing schemes that lead to additional switching events. As the opportunities brought by WBG devices, the higher blocking voltage of SiC devices enables these topologies to be implemented in higher-voltage systems, and the lower switching loss of WBG devices moderates the increased switching loss from utilizing additional switching events. These points are supported by a quantified case study on a 1.2 kV 4L-ANPC multilevel converter employing SiC power modules, for which a prototype has been built and experimentally tested in a downscaled 1 kV rig as proof of concept.

The authors hope this work can inspire reconsideration and reassessment of these simplified multilevel topologies in the new era of WBG power devices.

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